REMARKS

Claims 1-12 are pending in the application.

Claims 1-2 and 4-12 have been rejected.

Claims 1-12 have been amended as set forth herein.

Claims 13-20 have been added herein.

Claims 1-20 remain pending in this application.

Reconsideration of the claims is respectfully requested. The Applicants make the aforementioned amendments and subsequent arguments to place this application in condition for allowance. Alternatively, the Applicants make these amendments and offer these arguments to properly frame the issues for appeal. In this Response, the Applicants make no admission concerning any now moot rejection or objection, and affirmatively deny any position, statement or averment of the Examiner that was not specifically addressed herein.

I.   ALLOWABLE SUBJECT MATTER

The Examiner objected to Claim 3 as being dependent upon a rejected base claim, but suggested that Claim 3 would be allowable if it were rewritten in independent form including all the limitations of the base and intervening claims. Applicants thank the Examiner for this suggestion but elect not to rewrite Claim 3 at this time.

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II.   CLAIM REJECTIONS -- 35 U.S.C. § 103

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,286,599 in view of U.S. Patent No. 5,986,599. The Applicants respectfully traverse the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to

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modify the reference or to combine reference teachings. Second, there must be a reasonable

expectation of success. Finally, the prior art reference (or references when combined) must teach or

suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's

disclosure. MPEP § 2142. In making a rejection, the examiner is expected to make the factual

determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966),

viz., (1) the scope and content of the prior art; (2) the differences between the prior art and the claims

at issue; and (3) the level of ordinary skill in the art. In addition to these factual determinations, the

examiner must also provide "some articulated reasoning with some rational underpinning to support

the legal conclusion of obviousness." (*In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed.

Cir 2006) (cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385,

1396 (2007)).

Independent Claim 1 recites a communications receiver that includes a pulse detection unit,

for detecting pulses in a received signal. The pulse detection unit includes:

> a plurality of comparators;
> a sampling time generator configured to generate timing
> signals indicative of a plurality of sampling time points within a
> received pulse; and
> a reference level generator configured to generate a plurality
> of reference levels,
> wherein each of the comparators is programmable with a
> sampling time point selected from said plurality of sampling time
> points and with a reference level selected from said plurality of
> reference levels, and

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> wherein the received signal is applied to each of the comparators such that each of the comparators is configured to produce a respective output signal based on a comparison between the received signal level and the selected reference level at the selected sampling time point.

The Applicants submit that *Cheah* and *Matsuo*, alone or in combination, do not teach or suggest the aforementioned features of Claim 1. In particular, it is submitted that *Cheah* does not teach or suggest "a sampling time generator configured to generate timing signals indicative of a plurality of sampling time points." Accordingly, without conceding the propriety of the asserted combination, the asserted combination is likewise deficient.

The Office Action contends that *Cheah* (Figure 4, sample and hold circuits 60 and 62; and col. 2, lines 57-60) teaches a sampling time generator for generating signals indicative of a plurality of sampling time points. (*Office Action*, page 2). The Office Action argues that the pair of sample and hold circuits are configured to store the established signal amplitude levels. (*Office Action*, page 2). The Summary section cited by the Office Action, *Cheah* states:

> In one embodiment, the communication system also includes a receiver configured to receive RF transmissions in the frequency spectrum between 3.1 GHz and 10.6 GHz, according to a selected filter channel. The receiver may share the Gaussian filter with the transmitter and is configured to provide a data output along with a confidence level output indicative of a likelihood of error in the data output. The data output and the confidence level output may be provided through a pair of comparators which operate to <u>measure received RF transmissions against established signal amplitude levels</u> for logic 1s logic 0s in a received pulse train. <u>A pair of sample and hold circuits are configured to store the established signal amplitude levels</u>. (*Cheah*, col. 2, lines 48-60) (Emphasis Added)

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Cheah however, further describes the operation of the sample and hold circuits:

> Within the signal decision block 42, the detected signal from the RF detector 40 is clocked (by the bit timing clock 50) into two sample and hold (S/H) circuits. The `Hi` S/H circuit 60 is triggered by the presence of an RF pulse, and <u>it samples and holds the value (i.e., the signal amplitude) of the detected RF pulse</u>. On the other hand, the `Lo` S/H circuit 62 is triggered by the absence of an RF pulse. <u>It samples and holds the value of the RF signal in the absence of a pulse</u>. This value will represent the noise floor of the receiver. (*Cheah*, col. 9, lines 58-66) (Emphasis Added)

As shown here, *Cheah* only teaches that the sample and hold circuits are configured to sample and hold a value (i.e., the established signal amplitude) of a detected RF pulse. The output of the "Hi" S/H circuit (60) holds the signal amplitude of a detected RF pulse (*Cheah* col. 9, lines 60-63) and the output of the "Lo" S/H circuit (62) holds the signal amplitude of the RF signal in the absence of a pulse (*Cheah* col. 9, lines 63-67). The S/H circuits (60 and 62) are thus not generating timing signals and cannot be considered a sampling time generator. *Cheah* does not teach that either sample and hold circuits (60 and 62) can generate <u>timing signals indicative of a sampling time points within a received pulse</u>.

The Bit clock signal (50) may be considered as a timing generator. However, this Bit clock signal is synchronized with the detected input signal (see *Cheah* Fig. 5) and has a frequency equal to the frequency of the received input pulses. This is illustrated in Fig. 2 of *Cheah*, which shows that with every incoming data pulse (i.e. a 1 or a 0 of Data 12) corresponds a pulse of the Bit clock 14. In *Cheah* there are thus no "timing signals indicative of a plurality of sampling time points within a received pulse" but, in contrast, there is one single "timing signal" within a received pulse.

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In this respect, the Office Action is also referring to col. 2, lines 57-60 of *Cheah*. This cited passage in *Cheah* explains that the reference level of a logic 1 and of a logic 0 is set ("established") on the basis of the preamble of a signal packet. This setting is done by the S/H circuits (60 and 62) in combination with the comparators (64 and 66); incoming signals are then compared in the integrator circuits (68a-68e) in order to determine whether further incoming signals (the pulses of the packet after the preamble) correspond to a "1" (detected by 68e) or a "0". There is no reference to any "time generator" in this passage.

In addition, *Cheah* does not teach or suggest a reference level generator configured to generate "a plurality of reference levels" as recited in Claim 1. The Office Action again argues that the sample and hold circuits (60 and 62) and column 2, lines 57-60 teaches this element of Claim 1. *Cheah*, however, only teaches that the sample and hold circuits (62) is configured to sample and hold a value (i.e., the signal amplitude) in the absence of a pulse; thus representing a reference floor. *Cheah* contains no teaching that either sampling and hold circuit (60 and 62) can generate a plurality of reference levels.

Further, *Cheah* does not teach or suggest wherein "the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on a comparison between the received signal level and the selected reference level at the selected sampling time point" as recited in Claim 1. The Office Action contends that column 2, lines 55-60 teaches this element of Claim 1. *Cheah* further describes the operation of the comparators at column 10, lines 1-23, which states:

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Two comparators 64 and 66, which are each coupled to receive the outputs of the S/H circuits 60 and 62, compare the different voltage or current values representing the presence or absence of the RF pulses. In essence, these comparators now have the differential value of the detected signal with respect to the noise floor of the receiving system. The sample and hold circuits 60 and 62 perform these measurements during the preamble period of the transmission and hold these values for later reference. That is, the reference values are provided to the receiver for the balance of a transmission in order to allow the receiver to differentiate between logic "1s" and "0s" in the received pulse train.

One of the comparators, designated 64 in the diagram, is used to make a so-called "hard decision" (the data output 46) as to whether or not there is a detected pulse present in the received pulse train. This is accomplished by comparing the amplitude of the received signal against the known amplitude of the detected pulses received during the preamble period of the transmission. A bias weighting circuit can be provided to increase the sensitivity of this detection. A decision is then made as to whether or not there truly is a pulse (i.e., a logic "1") present in the detected signal, and this decision is termed the data `hard-decision`. (*Cheah*, col. 10, lines 1-23) (Emphasis Added)

Cheah, however, teaches that comparators (64 and 66) only receive two signals that are the voltage or current values from the sample and hold circuits (60 and 62), which are relied upon by the Office Action to teach the signals indicative of the plurality of sampling time points and plurality of reference levels. The output of S/H circuit (60) "holds the value (i.e., the signal amplitude) of the detected RF pulse" and the output of S/H circuit "will represent the noise floor of the receiver" (*Cheah* col. 9, lines 60-67); both outputs are thus depending on the received signal and cannot be considered to be "reference levels".

Cheah does not teach or suggest "the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on a comparison between the received signal level and the selected reference level at the selected sampling time point" as recited in Claim 1. The comparators (64 and 66) do not produce an output signal based on a comparison between the received signal level and the selected reference level at the selected sampling time point because there is no selected reference level available at the comparators as there is also not a selected sampling time point.

The Office Action concedes that *Cheah* does not disclose that the comparators are programmable with selected sampling time points. Nonetheless, the Office Action rejects Claim 1 contending that *Matsuo* provides this necessary disclosure. This contention respectfully is traversed.

In *Cheah*, the comparators (64 and 66) are not programmable with a sampling time point and with a selected reference level. The comparators do not have a "time" input and the input reference level used by the comparators (the + or − input) is given by the corresponding output of the S/H circuits, without any selection possibility.

Matsuo relates to a voltage comparator for an analog-to-digital converter and is provided for its alleged teaching of a comparator programmable with a sampling time point selected from a plurality of sampling time pints and with a reference level selected from a plurality of reference levels. (*Office Action*, page 3). The Office Action argues that *Matsuo* (col. 6, lines 13-17) teaches this element of Claim 1. The cited passage of *Matsuo* discloses a differential type voltage comparator used in AD converters. According to *Matsuo*, this differential type voltage comparator

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comprises a plurality of voltage comparators "for performing a sampling operation and a comparison operation" (*Matsuo*, col. 6, lines 12-13). The sampling operation according to *Matsuo* does not include the selection from a plurality of sampling time points and also not the programming of such selection. The sampling operation means only that a signal is sampled at regular time intervals. The comparison operation means that the successive samples of the input signal are compared with successive reference signals. There is no indication in *Matsuo* that the comparators can be programmed with reference signals. *Matsuo* does not teach or suggest "wherein each of the comparators is <u>programmable with a sampling time point</u> selected from said plurality of sampling time points and with a reference level selected from said plurality of reference levels." Therefore, *Matsuo* does not provide a disclosure that remedies the conceded deficiencies of *Cheah*.

For at least these reasons, the combination of *Cheah* and *Matsuo* fails to teach or suggest each and every feature of Claim 1 and its dependent claims. For similar reasons, *Cheah* and *Matsuo* fail to teach or suggest each and every feature Claim 7 and its dependent claims.

Accordingly, the Applicants respectfully request that the § 103 rejections with respect to Claims 1 and 7, and their respective dependent claims, be withdrawn.

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III.   NEW CLAIMS

The Applicants have added new Claims 13-20. The Applicants respectfully submit that no new matter has been added. At a minimum, the Applicants respectfully submit that Claims 13-20 are patentable for one or more reasons discussed above. The Applicants respectfully request entry and full allowance of Claims 13-20.

CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining Claims in the Application are in condition for allowance, and respectfully request an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckcarter.com.*

The Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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